Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising:

an interconnect;

a plurality of processor nodes, coupled to the interconnect, each processor node comprising:

at least one processor core, each processor core having an associated memory cache for caching memory lines of information;

~~an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information; and~~

~~a protocol engine implementing a predefined cache coherence protocol; and~~

a plurality of input/output nodes~~,~~ coupled to the interconnect; and~~, each input/output node including:~~

~~no processor cores;~~

~~an input/output interface for interfacing to an input/output bus or input/output device;~~

~~a memory cache for caching memory lines of information;~~

~~an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information; and~~

~~a protocol engine implementing the predefined cache coherence protocol~~

wherein the processor nodes and the input/output nodes collectively comprise a plurality of system nodes, each of which comprises:

input logic for receiving a first invalidation request, the invalidation request identifying a memory line of information and including a pattern of bits for identifying a subset of the plurality of system nodes that potentially store cached copies of the identified memory line; and

processing circuitry, responsive to receipt of the first invalidation request, for determining a next node identified by the pattern of bits in the invalidation request and for sending to the next node, if any, a second invalidation request corresponding to the first invalidation request, and for invalidating a cached copy of the identified memory line, if any, in the particular node of the computer system.~~.~~

2.-8. (Canceled).

9. (Currently amended) A computer system, comprising:

a plurality of multiprocessor nodes, each multiprocessor node comprising:

a multiplicity of processor cores, each processor core having an associated memory cache for caching memory lines of information;

~~an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information; and~~

~~a protocol engine implementing a predefined cache coherence protocol; and~~

a plurality of input/output nodes coupled to the plurality of multiprocessor nodes; and~~, each input/output node including:~~

~~no processor cores;~~

~~an input/output interface for interfacing to an input/output bus or input/output device;~~

~~a memory cache for caching memory lines of information;~~

~~an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information; and~~

~~a protocol engine implementing the predefined cache coherence protocol.~~

wherein the multiprocessor nodes and the input/output nodes collectively comprise a plurality of system nodes, each of which comprises:

input logic for receiving a first invalidation request, the invalidation request identifying a memory line of information and including a pattern of bits for identifying a subset of the plurality of system nodes that potentially store cached copies of the identified memory line; and

processing circuitry, responsive to receipt of the first invalidation request, for determining a next node identified by the pattern of bits in the invalidation request and for sending to the next node, if any, a second invalidation request corresponding to the first invalidation request, and for invalidating a cached copy of the identified memory line, if any, in the particular node of the computer system.

10.-16. (Canceled).

17. (New) The system of claim 1 wherein the system is reconfigurable so as to include any ratio of processor nodes to input/output nodes so long as a total number of processor nodes and input/output nodes does not exceed a predefined maximum number of nodes.

18. (New) The system of claim 1 wherein each processor node and input/output node further comprises a protocol engine implementing a predefined cache coherency protocol, wherein the protocol engine of each processor node is functionally identical to the protocol engine of each input/output node.

19. (New) The system of claim 9 wherein the system is reconfigurable so as to include any ratio of multiprocessor nodes to input/output nodes so long as a total number of multiprocessor nodes and input/output nodes does not exceed a predefined maximum number of nodes.

20. (New) The system of claim 9 wherein each multiprocessor node and input/output node further comprises a protocol engine implementing a predefined cache coherency protocol, wherein the protocol engine of each multiprocessor node is functionally identical to the protocol engine of each input/output node.